# The temperature mobility degradation influence on the zero temperature coefficient of Ellipsoidal MOSFET

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***Abstract*—The zero temperature coefficient (ZTC) is investigated by the simple model and three-dimensional numerical simulations in the Metal-Oxide-Semiconductor (MOS) Field Effect Transistor (MOSFET) with the ellipsoidal (EM) and conventional rectangular gate geometries (CM), considering the same channel widths (W), gate areas ($A_G$) and bias condition (BC) technology. A simple model is used to study the behavior of the gate voltage at ZTC ($V_{ZTC}$) in the linear and the saturation region. The influence of the temperature mobility degradation on $V_{ZTC}$ is analyzed for EM and CM devices. The $V_{ZTC}$ changes in the temperature range investigated showed a temperature mobility degradation dependence and the both devices showed the same behavior. The analysis takes into account temperature dependence model parameters such as threshold voltage and mobility. The analytical predictions are in very close agreement with experimental results in spite of the simplification used for the $V_{ZTC}$ model as a function of temperature in the linear and the saturation region.**

***Keywords— Zero temperature coefficient, Ellipsoidal layout style, Simple model, Mobility degradation.***

## I. INTRODUCTION

The environment temperature (T) variation has become an increasingly important factor as the continuing scaling of Complementary Metal-Oxide-Semiconductor (CMOS) technologies brings more integration in an integrated circuit (IC). Because, the changes in environment temperature, combined with non-uniform temperature inside these ICs, influences the reliability, electrical performance and functionality of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) [1]. Therefore, it is of fundamental importance to reduce more and more the dependence of the variation of a wide range of temperature in CMOS ICs. One of the possible solutions for the stable CMOS IC operation over a wide range of temperature is based in in electrical parameter from MOSFET named Zero Temperature Coefficient (ZTC).

The ZTC condition of a MOSFET, by definition, is the voltage gate ($V_{GS}$) which ensures that the drain current ($I_{DS}$) does not present change with the environment temperature variation ($dI_{DS}/dT = 0$), i.e., this condition defines a bias point of MOSFET in which its $I_{DS}$ presents small temperature sensitivity. This condition happens from the mutual cancelation of mobility of mobile charge carriers and threshold voltage ($V_{th}$) dependencies on temperature in a MOSFET, which it results in a ZTC bias point [2]. However, the mobility of mobile charge carriers compensation is sometimes not enough to satisfy stability in the ZTC point bias in a MOSFET [3].

There are some scientific works that model the behavior of $V_{GS}$ at ZTC point in the linear and saturation regions for the standard MOSFET (rectangular gate layout style) [4, 5, 6]. However, there is no modeling of $V_{GS}$ at ZTC point in MOSFETs implemented with different non-standard gate layout styles (Hexagonal/Diamond [7], Octagonal [8] and Ellipsoidal [9] MOSFETs).

Therefore, this paper focuses on the ZTC point behavior of MOSFET implemented with ellipsoidal gate layout style (Ellipsoidal MOSFET, EM) and it studies the influence of the temperature mobility degradation factor (c) on $V_{GS}$ at ZTC point in EM in relation to the standard MOSFET (Conventional MOSFET, CM), regarding the same gate area ($A_G$), channel width (W) and bias. This new model has been performed by three-dimensional (3D) numerical simulations data when the devices are operating in the linear and saturation regions.

It is expected that the mutual compensation of the mobility and the threshold voltage temperature dependences may result in a ZTC bias point for Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFETs). However, this mobility compensation is sometimes not enough to satisfy stability in the ZTC point bias [3].

The goal of this work is to study the influence of the temperature mobility degradation factor (c) on the bias gate voltage at the ZTC point in the ellipsoidal layout style for MOSFETs (EM) in relation to the typical rectangular one (CM) in both the linear and the saturation region by using a simple model. Three-dimensional (3D) numerical simulations data results are used to validate the model.

## II. THE ELLIPSOIDAL LAYOUT STYLE FOR PLANAR MOSFETS

Fig. 1 shows the three-dimensional (3D) structure of the EM. Note that the EM can be represented electrically by a parallel association of MOSFETs with different channel lengths $L_i = 2.\mathbf{x}$, $L_i = B.\ [1\text{-}4\ (y^2 / W^2)]^{1/2}$, where $b \leq L_i \leq B$.

So, the EM aspect ratio ($W / L_{eff\_EM}$) can be obtained by equation (1) [11]. Note that x 'and y' are the coordinates in the Cartesian plane of point P and have the same channel width

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(dy), as shown in Fig. 1 [10].

$$L_{eff\_EM} = \frac{b}{arcsin\left(\sqrt{1-\frac{b^2}{B^2}}\right)} \quad (1)$$

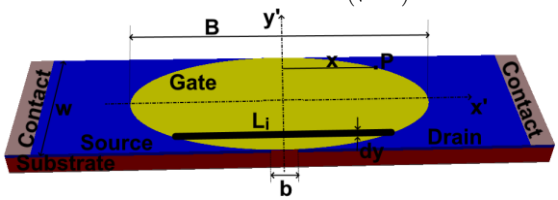


Fig.1 - The three-dimensional (3D) structure of the EM

When B=4L/$\pi$, where L is the conventional MOSFET channel length, EM and CM with the same W and $A_G$ [7]. Table I shows the dimensions of the EMs and CMs, $A_G$, $L_{eff}$_EM and the Leff_EM reductions in relation to the L of the CMs, which correspond to the drain current gain ($I_{DS}$) of the EM in relation to those of the corresponding CMs, due to the PAMDLE effect [9].

The Table 1 shows the reductions of the EM $L_{eff}$ in relation to those found in the counterparts of the CM, due to the PAMDLE effect.

TABLE I. GEOMETRIC CHARACTERISTICS OF THE STRUCTURES OF THE EMS AND THE SIMULATED CMS.

| | CM: | | | EM: | | | | (Leff-L)/L |
|---|---|---|---|---|---|---|---|---|
| # | W [μm] | L=Bπ/4 [μm] | $A_G$ [μm$^2$] | W [μm] | b [μm] | B [μm] | $L_{eff}$ [μm] | (x100) [%] |
| 1 | 5.95 | 7.00 | 41.65 | 5.95 | 1.05 | 8.913 | 6.14 | -12.3 |
| 2 | 5.95 | 9.97 | 59.35 | 5.95 | 1.05 | 12.701 | 8.53 | -14.4 |
| 3 | 5.95 | 11.97 | 71.22 | 5.95 | 1.05 | 15.241 | 10.15 | -15.2 |

Fig. 2a shows a top plan view of the EM structure. Note that, b and B are, respectively, the smallest and the longest channel length of the EM, W is the width of the channel and $E_1$, $E_2$ and $E_3$ are the components of the Longitudinal Electric Field (LEF) vectors due to the polarization of the drain ($V_{DS}$) [9-11].

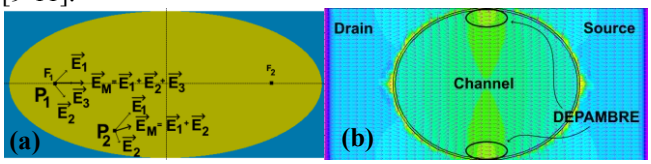


Fig.2 – (a) The top plan view of the EM structure (b) The behavior of the lines resulting from the LEF in the longitudinal section plane inside the channel of the EM structure operating in the saturation region.

$E_M$ is the resulting vector at a point located on the axis formed by the focus of the ellipse ($F_1$ and $F_2$) and is equal $E_1$+$E_2$+$E_3$. Note that for any other point located outside the axis formed by the focus of the ellipse, $E_M$ is equal to $E_1$+$E_2$ [X1]. Thus, it can be observed that the EM presents a resultant of the longitudinal electric field larger than that found in the conventional MOSFET which presents only one LEF vector in the region of the channel [1], considering the same gate area ($A_G$) and bias conditions (BC). This effect is known as the Longitudinal Corner Effect (LCE) [9-11].

Fig. 2b shows the behavior of the lines resulting from the LEF in the longitudinal section plane inside the channel of the EM structure operating in the saturation region. Note that the resulting LEF lines are curved in the Bird's Beak Regions. These regions have parasitic MOSFETs. Thus, due to this effect, EMs are more robust to Parasitic MOSFETs in the Bird's Beak Regions. This effect is known as Deactivation of Parasitic MOSFETs in the Bird's Beak Regions (DEPAMBBRE) [12].

Therefore, LCE, PAMDLE and DEPAMBBRE, found in EM, are able to increase the performance of EMs in relation to their counterpart CMs (same W and $A_G$).

## III. ZTC ANALYTICAL MODEL

The ZTC point is defined by the gate voltage ($V_{GS}$) that can be applied in MOSFET, in which ensures that its drain current ($I_{DS}$) remains constant with temperature variations [3]. Considering that a MOSFET operates at two different temperatures, T1 and T2, respectively, we observe that it generates two different electrical behaviors of $I_{DS}$ as a function of $V_{GS}$. When we plot these curves in the same graphic, we notice that they intersect at a point P, entitled of the "Zero Temperature Coefficient (ZTC) point", in which defines a specific $V_{GS}$, named $V_{ZTC}$, and a specific $I_{DS}$, named $I_{ZTC}$ and $I_{DS1}$ and $I_{DS2}$ are drain current at temperature T1 and T2 respectively, as illustrated in Figure 3.

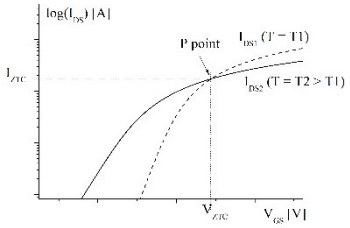


Fig.3 - The ZTC point defined by two characteristics curves of a MOSFET operating in two different temperatures, T1 and T2, respectively.

A simple analytical model, entitled Camillo-Martino ZTC[4], was developed for ZTC point in order to evaluate the electrical behavior of $V_{ZTC}$ as a function of temperature T2, considering the value of the threshold voltage at a known temperature T1 ($V_{th1}$) and also for a particular drain bias ($V_{DS}$) [4]. Thus, we can determine the value of $V_{ZTC}$ of a MOSFET operating in the linear region (as a resistor), regarding a specified temperature T2 ($V_{ZTC\ LIN}$) and $V_{DS}$, by using Equation (2) [4].

$$V_{ZTC\ LIN} = \frac{V_{th1}-\left(\frac{T_1}{T_2}\right)^c\left(V_{th1}+\frac{dV_{th}}{dT}(T_2-T_1)\right)}{1-\left(\frac{T_1}{T_2}\right)^c} + n\frac{V_{DS}}{2} \quad (2)$$

where n is the body factor and c is the mobility degradation factor of a particular temperature T2 [4], and is given by Equation (3)[13].

$$\mu_{n2} = \mu_{n1}\left(\frac{T_1}{T_2}\right)^c \quad (3)$$

Analogously, the value of $V_{ZTC}$ of a MOSFET operating in the saturation region (as an amplifier), regarding a specified temperature T2 ($V_{ZTC\ SAT}$), can be calculated by using Equation (4) [14]:

$$V_{ZTC\ SAT} = A + (A^2 - B)^{1/2} \quad (4)$$

where

$$A = \frac{V_{th1}-\left(\frac{T_1}{T_2}\right)^c\left(V_{th1}+\frac{dV_{th}}{dT}(T_2-T_1)\right)}{1-\left(\frac{T_1}{T_2}\right)^c} \quad (5)$$

$$B = \frac{{V_{th1}}^2-\left(\frac{T_1}{T_2}\right)^c\left(V_{th1}+\frac{dV_{th}}{dT}(T_2-T_1)\right)^2}{1-\left(\frac{T_1}{T_2}\right)^c} \quad (6)$$

The threshold voltage in the linear region was derived by the linear extrapolation method, where the threshold voltage corresponds with the gate voltage axis intercept of the linear extrapolation of the $I_{DS}$–$V_{GS}$ characteristics at its maximum first derivative (slope) point [15]. In the saturation region the threshold voltage was extracted by the ratio method (RM), which determines the gate voltage axis intercept of the ratio of the drain current to the square root of the transconductance [16]. This model [4] was evaluated to SOI nMOSFETS devices, however this work it is found to Ellipsoidal MOSFET devices.

## IV. RESULTS AND DISCUSSION

Three-dimensional (3D) numerical simulations were performed to obtain the characteristics curves of $I_{DS}$ as a function of $V_{GS}$ of EM and CM over the temperature range from 300 up to 550 K. The numerical models used in these simulations were: transverse electric field (Shirahata), low field mobility (Klaassen) and recombination effects (Shockley-Read-Hall) models [18].

Fig. 4 illustrates the values of $V_{ZTC\ LIN}$ of CM (Fig. 4a) and EM counterpart (Fig. 4b) as a function of the temperature T2, regarding T1 equal to 300K (27 ºC), p-type doping concentration ($N_A$) equal to $1.7x10^{17}$ cm$^3$, n-type drain/source doping concentration ($N_D$) equal to $1x10^{20}$ cm$^3$, thin gate-oxide thickness ($t_{ox}$) equal to 14.2 nm and for different c values.

The figure clearly shows for both device types that when the temperature coefficient (c) of the mobility increases, the $V_{ZTC}$ decreases. The temperature dependence of the threshold voltage in MOSFETs has been modeled in [19] and results, in

$$\frac{dV_{th}}{dT} = \frac{d\emptyset_F}{dT}\left[1 + \frac{q}{C_{ox}}\sqrt{\frac{\varepsilon_{Si}\,Na}{kT\,ln(Na/ni)}}\right] \quad (7)$$

In the linear region, Eq. (2) shows that when the temperature increases, $(dV_{th}/dT)(T2 - T1)$ increases and $[T1/T2]^c$ decreases. The competition of these two terms depends on the value of the c coefficient, which is responsible for the $V_{ZTC}$ changes as a function of temperature. The variation of $V_{ZTC}$ in EM and CM devices from 350 to 550K shown in Fig. 4 is summarized in Table 2.

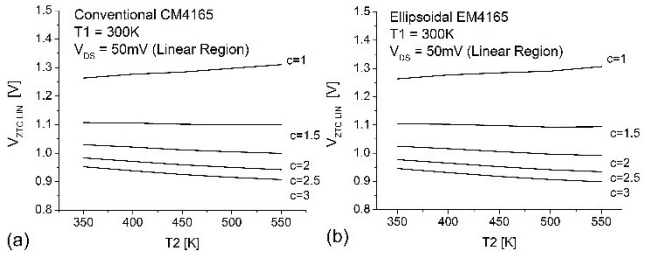


Fig. 4 - $V_{ZTC}$ of CM (a) and EM (b) MOSFETs devices operating in the linear region as a function of temperature for c varying between 1 and 3.

The $V_{ZTC\ LIN}$ variation from 350 to 550K in EM devices is the same than in CM ones, the variation in $V_{th}(T)$ depends on the Fermi level variation and also a function of the depletion region decrement as shown in Eq. (7).

The same analysis performed for the saturation region, with $V_{ZTC\ SAT}$ for T1 = 300K in function of T2 and using c as a parameter for EM and CM nMOSFETs leads to Fig. 5, based on Eqs. (4), (5) and (6). As shown in Fig. 5, when the temperature coefficient (c) of the mobility increases, the $V_{ZTC}$ decreases for both types of devices.

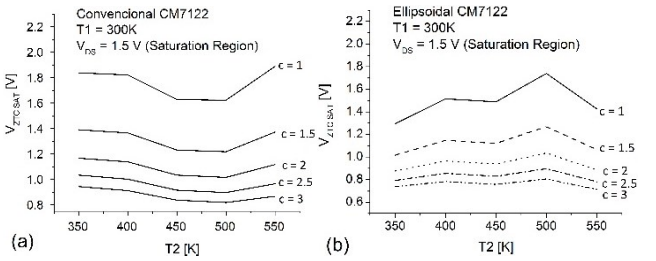


Fig. 5 $V_{ZTC}$ of CM (a) and EM (b) MOSFETs devices operating in the saturation region as a function of temperature for c varying between 1 and 3.

The slope of $V_{ZTC}$ versus T2 in function of the c factor is for CM and EM are shown in Fig. 6a and Fig. 6b for the linear and saturation operating region, respectively. For CM devices the $dV_{ZTC}/dT$ is near zero in the linear region for $c \approx 1.42$ and $c \approx 1.88$ in the saturation region. However, for EM ones this occurs for $c \approx 1.39$ in the linear region and $c \approx 2$ in the saturation region.

Using the proposed simple model [4], given by Eqs. (2) and (4), is analyzed the sensitivity of the $V_{ZTC}$ in function of $N_a$ and $t_{ox}$ variations, considering that the target is $N_a = 1.7x10^{17}$ cm$^{-3}$ and $t_{ox} = 14.2$ nm, adopted as a reference. The $\Delta V_{ZTC}$ is defined as

$$\Delta V_{ZTC} = V_{ZTC}(N_a; t_{ox}) - V_{ZTC}\ (\text{reference}) \quad (7)$$

Tables 3 show the results for EM devices in linear and saturation region, respectively. As can be seen the maximum error in $\Delta V_{ZTC}$ strongly depends on the introduced difference in $N_a$ and $t_{ox}$ values. However, a bigger variation in $\Delta V_{ZTC}$ occurs when the variation in $t_{ox}$, due to its influence on the $V_{th}$ value.

The aim of the analysis was to study the impact of introducing an error of +10% on the reference $N_a$ and $t_{ox}$. Table 3 shows that the maximum error observed for EM devices is 11.2% in the linear region and 9.8% in the saturation region, respectively.

TABLE II: MAXIMUM VARIATION OF $V_{ZTC}$ BIAS IN THE TEMPERATURE RANGE 350K-550K.

| $V_{ZTC}$(300K) – $V_{ZTC}$(550K) | | | | | | |
|---|---|---|---|---|---|---|
| | *CM (mV)* | | | *EM (mV)* | | |
| ***c*** | ***4165*** | ***5935*** | ***7122*** | ***4165*** | ***5935*** | ***7122*** |
| 1 | 47 | 62 | 65 | 43 | 51 | 40 |
| 1.5 | -8 | 1 | 3 | -10 | -6 | -12 |
| 2 | -31 | -25 | -23 | -33 | -29 | -34 |
| 2.5 | -41 | -38 | -36 | -43 | -40 | -44 |
| 3 | -45 | -43 | -41 | -47 | -45 | -48 |

Analyzing Fig. 7a and Fig. 7b, $V_{ZTC}$ for EM and CM are both approximately equal to 1.0V and 1,2V, for a $V_{DS}$ equal to 50 mV (Linear) and 1.5V (Saturation), respectively. The simple fact that $V_{ZTC}$ are the same between Ellipsoidal layout (EM) style and rectangular layout (CM) style, according to each manufacturing technology, confirming the identical trends of $V_{th}$ and the mobility of the mobile charge carriers with the temperature [20-22].

TABLE III: SENSITIVITY OF THE PROPOSED METHOD BY ANALYSIS OF THE VARIATION IN $\Delta V_{ZTC}$ WITH A 10% CHANGE IN $N_A$ AND $T_{OX}$ VALUES FOR EM DEVICES OPERATING IN THE LINEAR AND THE SATURATION REGION.

| **EM** | | **Error in $\Delta V_{ZTC}$ (%)** | |
|---|---|---|---|
| ***$t_{ox}$ (nm)*** | ***Na ($10^{17}$ cm$^{-3}$)*** | ***Linear*** | ***Saturation*** |
| 12,78 | 1,7 | 11.2 | 9.8 |
| 14,2 | | reference | reference |
| 15,62 | | 10.2 | 9.4 |
| 14,2 | 1,53 | 4.1 | 4.3 |
| | 1,7 | reference | reference |
| | 1,87 | 5.1 | 3.4 |

However, ZTC current, $I_{ZTC}$, of the devices are different. The $I_{ZTC}$ for CM is equal to 0.6µA, while it is equal to 1.9µA for EM, which corresponds to 16,7% of gain in the linear region. In the saturation region, the $I_{ZTC}$ for CM is equal to 4.1µA, while it is equal to 13.2µA for EM, which corresponds to 22% of gain. These gains presented by EMs, are thanks to LCE and PAMDLE, which are able to boost EM $I_{DS}$, throughout the large temperature range that we considered.

## V. CONCLUSIONS

In this work a simple model to determine the ZTC point was used to investigate MOSFET in ellipsoidal (EM) and conventional rectangular gate geometries (CM), considering the same channel widths (W), gate areas ($A_G$) and bias condition (BC) over the temperature range from 300 up to 550K.

The $V_{ZTC}$ changes in the temperature range investigated showed a temperature mobility degradation dependence and the both devices showed the same behavior. The influence of the temperature coefficient (c) of the mobility on the ZTC bias point in EM and CM devices was also investigated using a simple model for the linear and saturation region.

The simple model simulations results showed that the temperature coefficient (c) of the mobility values on the ZTC bias point that does not cause variation in $V_{ZTC}$ are 1.39 for EM devices and 1.42 for CM ones in the linear region. For saturation region were found 2 for EM devices and 1.88 for CM ones. In both the cases, comparing results obtained by the simple model with simulations data, a good agreement is found in spite of the simplification used in the model.

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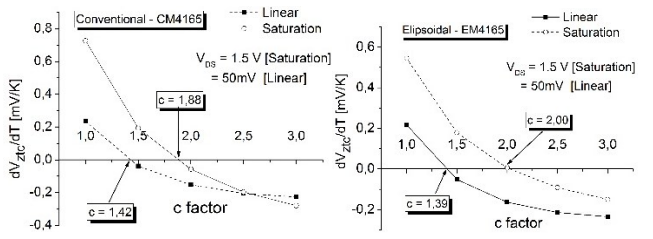


Fig.6 The slope of $V_{ZTC}$ bias versus the temperature T2 in function of the c factor for CM and EM devices in the linear and the saturation region.

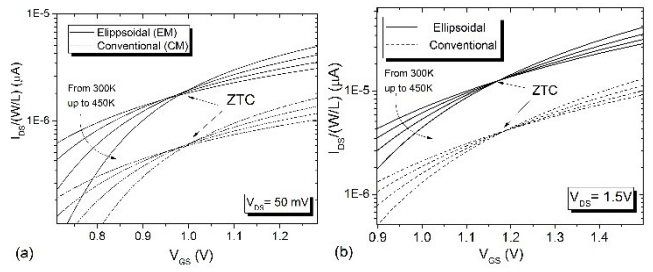


Fig. 7. Simulated curves of $I_{DS}$ as a function of $V_{GS}$ for different temperatures, highlighting ZTC point for EM and CM in the linear (a) $V_{DS}$ = 50mV and saturation (b) $V_{DS}$ = 1.5 V region.

## REFERENCES

[1] D. Wolpert, P. Ampadu, "Managing Temperature Effects in Nanoscale Adaptive Systems", Springer, 2012.

[2] Y. Q. Aguiar, A. L. Zimpeck, C. Meinhardt, and R. A. L. Reis, "Temperature dependence and ZTC bias point evaluation of sub 20nm bulk multigate devices," in Proc. 24th IEEE Int. Conf. Electron. Circuits Syst. (ICECS), vol. 2018, 2018, pp. 270–273, doi: 10.1109/ICECS.2017.8291999.

[3] I.M. Filanovsky, A. Allam, Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits, IEEE Trans. Circuits Syst. 48 (7) (2001) 876–884.

[4] L. M. Camillo et al., "The Temperature Mobility Degradation Influence on the Zero Temperature Coefficient of Partially and Fully Depleted SOI MOSFETs", Micr. Journal, vol. 37, 2006, 952-957

[5] C. Schneider, C. Galup-Montoro, "CMOS Analog Design Using All-Region MOSFET Modeling", 1st.ed. [S.l.]: Cambridge University Press, 2010.

[6] P. Toledo, H. Klimach, D. Cordova, S. Bampi, and E. Fabris, "Self-biased cmos current reference based on the ztc operation condition," in Integrated Circuits and Systems Design (SBCCI), 2014 27th Symposium on, Sept 2014, pp. 1–7.

[7] E. H. S. Galembeck, C. Renaux, J. W. Swart, D. Flandre, and S. P. Gimenez, "The impact of LCE and PAMDLE Regarding Different CMOS ICs Nodes and High Temperatures," IEEE J. Electron Devices Soc., vol. 9, no. April, 2021, doi: 10.1109/JEDS.2021.3071399.

[8] E. H. S. Galembeck, D. Flandre, C. Renaux, and S. P. Gimenez, "Digital Performance of OCTO Layout Style on SOI MOSFET at High Temperature Environment," J. Integr. Circuits Syst., vol. 14, no. 2, pp. 1–8, 2019, doi: 10.29292/jics.v14i2.34.

[9] S. P. Gimenez, M. M. Correia, E. D. Neto, and C. R. Silva, "An Innovative Ellipsoidal Layout Style to Further Boost the Electrical Performance of MOSFETs," IEEE Electron Device Letters, vol. 36, no. 7, pp. 705–707, 2015, doi: 10.1109/LED.2015.2437716.

[10] M. M. Correia and S. P. Gimenez, "Boosting the electrical performance of MOSFET switches by applying Ellipsoidal layout style," 2015 30th Symposium on Microelectronics Technology and Devices (SBMicro), Salvador, 2015, pp. 1-4. doi: 10.1109/SBMicro.2015.7298122.

[11] S. P., Gimenez, 'The Wave SOI MOSFET: A New Accuracy Transistor Layout to Improve Drain Current and Reduce Die Area for Current Drivers Applications', *ECS Trans*, Volume 19, Issue 4, Pages 153-158, 2009.

[12] L. Fino, D. Flandre, S.P. Gimenez, "Boosting the total ionizing dose tolerance of digital switches by using OCTO SOI MOSFET". IOP Semicond. Sci. Technol. 30, 105024 (2016).

[13] S. M., SZE, Physics of Semiconductor Devices. Wiley-Interscince Publication, 2a edição, ed. New York: J. Wiley & Sons, 1981.

[14] L. M. Camillo, J. A. Martino, E. Simoen and C. Claeys, Symposium on Silicon-on-Insulator Technology and Devices XII, The Electrochemical Soc. Ser. PV 2005-03, p. 289, (2005).

[15] D. Schroder, Semiconductor Material and Device Characterization. Wiley, New York, 1990.

[16] J. Liou et al., Analysis and Design of MOSFETs, Kluwer, Dordrecht, MA, 1998.

[17] S. P. Gimenez et. al., "Compact Diamond MOSFET model accounting for PAMDLE applicable down 150 nm node", Electronics Letters, vol. 50, no. 22, p. 1618-1620, Oct. 2014.

[18] ATLAS Users Manual, SILVACO International.

[19] G. Groeseneken, et al., Temperature dependence of threshold voltage in thin-film SOI MOSFET's, IEEE Trans. Electron Devices 11 (8) (1990) 329–331.

[20] J.-P. Colinge and C. A. Colinge, Physics of Semiconductor Devices, 2nd ed. Hoboken, NJ, USA: Wiley, 2002.

[21] D. Wolpert and P. Ampadu, Managing Temperature Effects in Nanoscale Adaptive Systems, New York, NY, USA: Springer, 2012.

[22] E. A. Gutiérrez-D., M. J. Deen, and C. Claeys, Low Temperature Electronics?: Physics, Devices, Circuits, and Applications. Cambridge, MA, USA: Academic, 2001.